IN THE SPECIFICATION:

Please amend paragraph **[0005]** as follows:

[0005] Chalcogenide material exhibits different electrical characteristics depending upon its state. For example, in its amorphous state, the material exhibits lower electrical conductivity than it does in its crystalline state. The operation of chalcogenide memory cells requires that a region of the chalcogenide memory material, called the chalcogenide active region, be subjected to a current pulse typically with a current density between about 10^5 and 10^7 amperes/cm^2 to change the crystalline state of the chalcogenide material within the active region contained within a small pore. This current density may be accomplished by first creating a small opening in a dielectric material that is itself deposited onto a lower electrode material. A second dielectric layer, typically of silicon nitride, is then deposited onto the dielectric layer into the opening. The second dielectric layer is typically about 40 Angstroms thick. The chalcogenide material is then deposited over the second dielectric layer and into the opening. An upper electrode material is then deposited over the chalcogenide material. Carbon is commonly used as the electrode material, although other materials have also been used, for example, molybdenum and titanium nitride. A conductive path is then provided from the chalcogenide material to the lower electrode material by forming a pore in the second dielectric layer by a ~~well-known~~ well-known firing process.

Please amend paragraph **[0009]** as follows:

[0009] The energy input required to adjust the crystalline state of the chalcogenide active region of the memory cell is directly proportional to the dimensions of the minimum ~~cross-sectional~~ cross-sectional dimension of the pore, e.g., smaller pore sizes result in smaller energy input requirements. Conventional chalcogenide memory cell fabrication techniques provide minimum cross-sectional pore dimension, diameter or width of the pore, that is limited by the photolithographic size limit. This results in pore sizes having minimum lateral dimensions down to approximately 0.35 microns. However, further reduction in pore size is desirable to achieve improved current density for writing to the memory cell.

Please amend paragraph **[0022]** as follows:

[0022] ~~FIG. 4(a)~~ FIG. 4a is a top plan view of a generally rectangular contact pattern formed from the resist material and silicon oxide layers;

Please amend paragraph **[0023]** as follows:

[0023] ~~FIG. 4(b)~~ FIG. 4b is a top plan view of a generally circular contact pattern formed from the resist material and silicon oxide layers;

Please amend paragraph **[0057]** as follows:

[0057] A contact pattern 108 is then etched in the resist material layer 106 and the silicon oxide layer 104 using conventional masking, exposing, etching, and photoresist stripping techniques, as shown in FIG. 3. The contact pattern 108 may be defined from the resist material layer 106 and silicon oxide layer 104, for example, as a generally rectangular block as shown in ~~FIG. 4(a),~~ FIG. 4a, or as a substantially circular block as shown in ~~FIG. 4(b).~~ FIG. 4b. The contact pattern 108 is preferably formed using a conventional contact hole mask, resulting in the substantially circular block shown in ~~FIG. 4(b).~~ FIG. 4b. The minimum lateral dimension of the contact pattern 108 preferably will be approximately 0.4 μm. The contact pattern 108 (see FIG. 3) includes a generally horizontal bottom surface 110 common to the conductive material layer 102, and generally vertical side walls 112 at its outer periphery.

Please amend paragraph **[00059]** as follows:

[0059] The portion of the conductive material layer 102 not covered by the silicon oxide layer ~~pattern~~ 104 is etched using wet etch or dry plasma etching techniques. The portions of conductive material layer 102 beneath silicon oxide layer ~~pattern~~ 104 being undercut to form a frustoconical shaped tip or protrusion 114 above the remaining exposed surface of the conductive material layer 102, as shown in FIG. 6. The frustoconical tip 114 preferably has a minimum frustum lateral dimension D of approximately 0.1 μm. The base of the tip 114 preferably will have a base minimum lateral dimension of approximately 0.4 μm, i.e., the same dimension as the lateral dimension of the contact pattern 108. The tip 114 will preferably have a height of

approximately 2000 Angstroms. The removal of the silicon oxide layer 104 is accomplished using conventional wet etch techniques, as shown in FIG. 7. The contact pattern 108 thus provides a means for defining the area of contact of the base of the frustoconical tip 114 of the conductive material layer 102 of about 0.00785 μm^2 [π x (0.05 μm)^2]. Although the above dimensions are given as "preferred," it is understood that a goal of the present invention is to form the tip 114 as small as possible while maintaining uniformity and dimensional control.

Please amend paragraph **[0070]** as follows:

[0070] In a particularly preferred embodiment, the methods described above are utilized to form an array 168 of chalcogenide memory cells 170 that are addressable by an X-Y grid of upper and lower conductors, i.e., electrodes, as shown in FIG. 22. In the particularly preferred embodiment, diodes are further provided in series with the chalcogenide memory cells to permit read/write operations from/to individual chalcogenide memory cells 170, as will be recognized by persons of ordinary skill in the art. Thus, the chalcogenide memory cells 170 can be utilized in a memory chip 172 which interacts with a ~~CPU (central processing unit)~~ central processing unit (CPU) 174 within a computer 176, as schematically illustrated in FIG. 23.

Please amend paragraph **[0074]** as follows:

[0074] The portion of the conductive material layer 102 not covered by the silicon oxide layer ~~pattern~~ 104 is etched using wet etch or dry plasma etching techniques. The portions of conductive material layer 102 beneath silicon oxide layer ~~pattern~~ 104 being undercut to form a sharp tip 180 above the remaining exposed surface of the conductive material layer 102, as shown in FIG. 29. The silicon oxide layer ~~pattern~~ 104 is then removed, as shown in FIG. 30. A layer of insulative material 116 is deposited onto the conductive material layer 102 to a level above the sharp tip 180, as illustrated in FIG. 31. The insulative material layer 116 is then preferably planarized using a conventional abrasive technique such as a chemical mechanical planarization (CMP) process, as illustrated in FIG. 32, to form the intermediate structure 160. The CMP process is performed to level and expose a top surface 182 of the sharp tip 180 formed on the conductive material layer 102. This method allows for greater control of a surface area of

top surface 182 of the sharp tip 180 by controlling the depth of the planarization. Once the intermediate structure 160 is formed, the chalcogenide memory cell may then be formed using the methods described above and shown in FIGS. 10-15 and FIGS. 16-21.